WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a fixed voltage generating circuit;

a first reference voltage generating circuit to form a first reference voltage by an amplifying circuit by receiving the fixed voltage formed with said fixed voltage generating circuit and adjusting the voltage gain with a resistance circuit and a switch controlled by a first trimming switch setting signal;

a first output buffer which is activated by a first control signal to form an internal voltage corresponding to said first reference voltage;

a second reference voltage generating circuit to form a second reference voltage by adjusting the combination of threshold voltages of MOSFETs with a plurality of MOSFETs and a switch controlled by a second trimming switch setting signal;

a second output buffer activated with a second control signal to form an internal voltage corresponding to said second reference voltage; and

an internal circuit to receive the internal voltage supplied from said first output buffer or said second output buffer activated by said first control signal and said second control signal,

wherein said internal circuit is set to the active condition by said first control signal when the internal

voltage is supplied from said first output buffer and to the standby condition by said second control signal when the internal voltage is supplied from said second output buffer.

2. The semiconductor integrated circuit device according to claim 1,

wherein said second reference voltage generating circuit includes: a plurality of serial circuits, each of which is comprised of a plurality of diode type MOSFETs and switches; and a current source circuit provided in common for a plurality of said serial circuits, and

wherein said second reference voltage is adjusted by controlling said switches with said second trimming setting signal.

3. The semiconductor integrated circuit device according to claim 1,

wherein said second reference voltage generating circuit includes: a constant voltage circuit to form a forward voltage of a PN junction diode; a plurality of cascade-connected voltage follower circuits which is given an offset voltage with a differential MOSFET which makes the currents of different current densities flow; and a selector to select the voltage at the cascade-connecting points of said differential amplifying circuit, and

wherein said constant voltage is used as an input

voltage of the initial stage circuit of said cascade-connected circuit, and said selector is controlled by said second trimming switch setting signal to output any one of said cascade-connecting points as said second reference voltage.

4. The semiconductor integrated circuit device according to claim 1, further comprising a third output buffer having the current supply capability lower than that of said first output buffer,

wherein said third output buffer is set to the operating condition in place of said first output buffer during the DC current testing condition of the semiconductor integrated circuit device.

5. The semiconductor integrated circuit device according to claim 4,

wherein said first output buffer is activated by said first control signal,

wherein said third output buffer is activated by a third control signal, and

wherein said fixed voltage generating circuit and said first reference voltage generating circuit are activated by a logical sum (OR) signal of said first control signal and said second control signal.

6. The semiconductor integrated circuit device according to claim 1, further comprising a voltage detecting circuit for detecting that an output voltage of said first control signal has reached the

predetermined voltage to assure the stable operation of said internal circuit,

wherein when said first fixed voltage generating circuit, first reference voltage generating circuit and first output buffer are shifted to the active condition from the non-active condition by said first control signal, supply of clock to said internal circuit is started by a detection signal of said voltage detection circuit, and the second output buffer is shifted to the non-active condition by said second control signal.

7. The semiconductor integrated circuit device according to claim 6, wherein said voltage detecting circuit includes a voltage comparing circuit to compare said fixed voltage with said first reference voltage and a delay circuit to receive the voltage comparison output, and said detection signal is formed by delaying, with said delay circuit, the comparison output signal indicating that said first reference voltage becomes higher than said fixed voltage.

8. The semiconductor integrated circuit device according to claim 1, further comprising a third output buffer which receives said second reference voltage and is activated by a fourth control signal,

wherein said fourth control signal activates said third output buffer under the condition that an internal voltage corresponding to said first reference voltage is outputted by said first control signal to make said

internal circuit to the operating condition, and said internal circuit forms said second trimming switch setting signal to set the output voltage of said third output buffer to the predetermined voltage and then store this signal to a non- volatile storage circuit included in the internal circuit.

9. The semiconductor integrated circuit device according to claim 8, wherein said internal circuit forms said first trimming switch setting signal so as to set the output voltage of said first output buffer to the predetermined voltage and then stores this signal to said non-volatile storage circuit.

10. The semiconductor integrated circuit according to claim 9,

wherein said internal circuit includes a microprocessor, a ROM storing at least a part of the operations of said microprocessor, and the non-volatile storage circuit, and

wherein said ROM includes a program to execute the operation to form the first trimming switch setting signal and the second trimming switch setting signal for setting said first reference voltage and the second reference voltage to the predetermined voltage and the operation to store such trimming switch setting signals to said non-volatile storage circuit.

11. The semiconductor integrated circuit device according to claim 9,

wherein said internal circuit includes a microprocessor, a ROM storing at least a part of the operations of said microprocessor, and the non-volatile storage circuit, and

wherein said ROM includes a function for reading a program for setting said first reference voltage and second reference voltage to the predetermined voltage.

12. A semiconductor integrated circuit device comprising:

a voltage generating circuit to form a first voltage;

a first reference voltage generating circuit including: an amplifying circuit having a first input terminal to receive said first voltage, a second input terminal, and an output terminal; a first resistance connected between said output terminal and said second input terminal; and a second resistance connected between said second input terminal and second voltage, said first reference voltage generating circuit forming a first reference voltage;

a first output buffer to form an internal voltage corresponding to said first reference voltage;

a second reference voltage generating circuit including: a first MOSFET of diode connection and a current source circuit which are connected in serial between said second voltage and a third voltage; and a second MOSFET having the gate connected to the node

between said first MOSFET and said current source circuit and outputting the second reference voltage from the source/drain path thereof;

a second output buffer to form an internal voltage corresponding to said second reference voltage; and

an internal circuit to receive the internal voltage supplied from said first output buffer and second output buffer,

wherein said internal voltage is supplied from said first output buffer when said internal circuit is in the active condition, and said internal voltage is supplied from said second output buffer when said internal circuit is in the standby condition.

13. A semiconductor integrated circuit device, comprising:

a voltage generating circuit to form a first voltage;

a first reference voltage generating circuit including: an amplifying circuit having a first input terminal to receive said first voltage, a second input terminal, and an output terminal; a first resistance connected between said output terminal and said second input terminal; and a second resistance connected between said second input terminal and a second voltage, said first reference voltage generating circuit forming a first reference voltage;

a second reference voltage generating circuit

including: a first MOSFET of diode connection and a current source circuit which are connected in serial; and a second MOSFET having the gate connected to the node between said first MOSFET and said current source circuit and outputting said second reference voltage from the source/drain path thereof; and

an internal circuit to operate with an internal voltage,

wherein said internal voltage is formed based on said first reference voltage and said second reference voltage,

wherein said first reference voltage generating circuit is in the active condition when said internal circuit is in the active condition, and

wherein said first reference voltage generating circuit is in the non-active condition and said second reference voltage generating circuit is in the active condition when said internal circuit is in the standby condition.

14. A semiconductor integrated circuit device comprising:

a first reference voltage generating circuit receiving said fixed voltage and including an amplifying circuit having a resistance circuit and a switch controlled by a first trimming switch setting signal, to form a first reference voltage;

a second reference voltage generating circuit

including a plurality of MOSFETs and a switch controlled by a second trimming switch setting signal, to form a second reference voltage; and

an internal circuit to operate by receiving an internal voltage;

wherein said internal voltage is formed based on said first reference voltage or second reference voltage,

wherein said first reference voltage generating circuit is in the active condition when said internal circuit is in the active condition, and

wherein said first reference voltage generating circuit is in the non-active condition and said second reference voltage generating circuit is in the active condition when said internal circuit is in the standby condition.